(n+1) signal and the conventional precharge signal. A set of three replacement sheets are appended to this Reply and Amendment. Accordingly, Applicants respectfully submit that the Examiner's objection to the drawings has been overcome

In the Claims

Amend claims 1-11 as follows:

1. (Currently Amended) A method for accessing memory cells within a ~~dynamic hardware memory block~~ memory array operated with a precharge mechanism, in which differential read and write access operations are performed by activating a true bitline and a complement bitline, the method comprising:

determining whether a next memory access operation occurring subsequent to a current access operation is a read access operation or a write access operation; and

performing a precharge of the true and complement bitlines only when a read access operation follows the current access operation.

2. (Currently Amended) The method according to claim 1, wherein the memory array comprises a static random access memory (SRAM) array ~~comprises the memory cells~~.

3. (Currently Amended) The method according to claim 1, in which a first precharge control signal is combined with a read cycle (n+1) control signal to evaluate whether a next memory access cycle comprises a read access or a write access.

4. (Original) The method according to claim 3, wherein the first precharge control signal and the read cycle n+1 control signal are combined to yield a second precharge signal.

5. (Original) The method according to claim 3, wherein the read cycle (n+1) control signal is asserted according to an operating mode of the memory array, such that a write access operation occurring over a plurality of system clock cycles results in a continuous assertion of the next read cycle (n+1) control signal until the write access operation is complete.

6. (Original) The method according to claim 3, wherein the read cycle (n+1) control signal is asserted two system clock cycles in advance of a next memory access operation during a delay between when an address of the memory array is specified and a current access operation is complete.

7. (Original) The method according to claim 3, wherein the next read cycle (n+1) control signal is asserted after a delay of one clock cycle during a period of time when no memory operation is performed.

8. (Original) An integrated circuit memory array adapted for low power operation, comprising:

a plurality of addressable memory cells arranged in rows and columns, the memory cells segmented into a plurality of memory blocks;

a plurality of column lines, each coupled to a corresponding column of memory cells;

a plurality of row lines, each coupled to a corresponding row of memory cells;

a precharge circuit coupled to the plurality of row lines, the precharge circuit provided to assert the plurality of row lines in a memory block to a high logic level following a memory access operation;

a first precharge signal controller coupled to the precharge circuit, the first precharge signal controller provided to generate a first precharge control signal;

a read cycle signal controller for generating a read cycle (n+1) signal when a next memory access operation is read access operation; and

a logic element to evaluate the first precharge control signal and the read cycle control (n+1) signal, the logic element asserting a second precharge control signal when a next memory access is a read access operation for controlling the precharge circuit.

9. (Original) The memory array according to claim 8, wherein the logic element comprises an AND gate.

10. (Original) The memory array according to claim 8, wherein the logic element comprises a multiplexer.

11. (Original) The memory array according to claim 8, wherein the memory array is a static random access memory (SRAM).

12. (New) The method according to claim 1, wherein the memory array comprises a dynamic random access memory (DRAM) array.